In the Claims:

Claim 1 (previously presented): An image transform processor for processing image data, comprising:

a programmable arithmetic processor capable of receipt of the image data from a data source over a data path and processing the digital image data, the programmable arithmetic processor comprising a first set of local buffers and a second set of local buffers, each buffer in the first set of local buffers alternately used for fetching input image data and each buffer in the second set of local buffers alternately used for storing output image data; and

a programmable input addresser that controls transfer of the image data from the data source to the programmable arithmetic processor by providing a source address onto a source address path, the source address identifying the data source.

Claim 2 (original): The image transform processor of claim 1, wherein the programmable input addresser further controlling transfer of the image data to the programmable arithmetic processor by providing a storage address to the programmable arithmetic processor, the storage address identifying a location within the programmable arithmetic processor for storage of the digital image data.

Claim 3 (original): The image transform processor of claim 1, wherein the data source being a frame capture processor, the source address identifying the frame capture processor.

Claim 4 (original): The image transform processor of claim 1, wherein the data source being a memory, the source address being a memory address identifying a location of the image data within the memory.

Claim 5 (previously presented): The image transform processor of claim 1, wherein the data source being a memory, the source address path being a read address bus coupled between the programmable input addresser and the memory, the source address being a memory address identifying a location of the digital image data within the memory.

Claim 6 (original): The image transform processor of claim 1, the storage location within the programmable arithmetic processor being a local buffer.

Claim 7 (canceled).

Claim 8 (original): The image transform processor of claim 1 further comprising:

a programmable output addresser controlling transfer of the image data from the programmable arithmetic processor to a memory by providing a write address onto a write path, the write address identifying a write address in the memory for storage of the digital image data.

Claim 9 (original): The image transform processor of claim 8, wherein the write path is a write address bus electrically connected to the programmable output addresser and the memory.

Claim 10 (original): The image transform processor of claim 8, wherein the programmable output addresser further controlling transfer of the image data by providing a retrieval address to the programmable arithmetic processor, the retrieval address identifying a location within the programmable arithmetic processor for retrieval of the image data.

Claim 11 (original): The image transform processor of claim 10, wherein the retrieval location within the programmable arithmetic processor is a buffer.

Claim 12 (original): The image transform processor of claim 10, wherein the retrieval location within the programmable arithmetic processor is at least one buffer of a plurality of buffers.

Claim 13 (previously presented): An image transform processor for processing image data, the image transform processor comprising:

a programmable arithmetic processor capable of receiving the image data from a memory over a data bus coupled between the programmable arithmetic processor and the memory and processing the image data, the programmable arithmetic processor comprising a first set of local buffers and a second set of local buffers, each buffer in the first set of local buffers alternately used for fetching input image data and each buffer in the second set of local buffers alternately used for storing output image data; and

a programmable input addresser controlling transfer of the digital image data from the

memory to the programmable arithmetic processor by:

(i) providing a memory address onto a read address bus coupled between the programmable input addresser and the memory, the memory address identifying a location of the image data within the memory, and

(ii) providing a storage address to the programmable arithmetic processor, the storage address identifying a local buffer within the programmable arithmetic processor for storage of the image data.

Claim 14 (previously presented): An image transform processor for processing image data, comprising:

a programmable arithmetic processor capable of receiving the image data from a memory over a data bus coupled between the programmable arithmetic processor and the memory and processing the image data, the programmable arithmetic processor comprising a first set of local buffers and a second set of local buffers, each buffer in the first set of local buffers alternately used for fetching input image data and each buffer in the second set of local buffers alternately used for storing output image data;

a programmable input addresser controlling transfer of the image data from the memory to the programmable arithmetic processor by:

(i) providing a memory address onto a read address bus coupled between the programmable input addresser and the memory, the memory address identifying a location of the image data within the memory, and

(ii) providing a storage address to the programmable arithmetic processor, the

storage address identifying a first local buffer within the programmable arithmetic processor for storage of the image data; and

a programmable output addresser controlling transfer of the image data from the programmable arithmetic processor to the memory by:

(i) providing a write address onto a write address bus coupled between the programmable output addresser and the memory, the write address identifying a write address in the memory for storage of the image data, and

(ii) providing a retrieval address to the programmable arithmetic processor, the retrieval address identifying a second local buffer within the programmable arithmetic processor for retrieval of the image data.

Claims 15-32 (cancelled).

Claim 33 (original): An image transform processor comprising:

a programmable input addresser to retrieve an image as a received image in accordance with a first programmed predefined access pattern, the programmable input addresser to output the received image in accordance with a second programmed predefined access pattern;

a programmable output addresser;

a SIMD processor including a controller coupled to a memory storing an at least one image processing instructions, the SIMD processor having a plurality of processing elements and a plurality of local buffers arranged in a plurality of levels and a plurality of processing banks, each processing bank in the plurality of processing banks being connected in parallel with

another processing banks in the plurality of processing banks, the controller being coupled to each processing element in the plurality of processing elements and each local buffer in the plurality of local buffers to control the operation of each processing element and each local buffer such that the plurality of processing banks simultaneously respond to an instruction from the controller, the SIMD processor being arranged as:

(i) a first level of the plurality of levels including a first set of local buffers from the plurality of local buffers;

(ii) a second level of the plurality of levels including a second set of local buffers from the plurality of local buffers;

(iii) a third level of the plurality of levels including a third set of local buffers from the plurality of local buffers;

(iv) a fourth level of the plurality of levels including a fourth set of local buffers from the plurality of local buffers;

(v) a processing level including a set of processing elements from the plurality of processing elements that generates a processed image from the image stored in the plurality of local buffers in accordance with an image processing instruction;

each processing bank including one local buffer of the first set of local buffers, one local buffer of the second set of local buffers, a processing element from the set of processing elements, one local buffer of the third set of local buffers, and one local buffer of the fourth set of local buffers, the processing element of each processing bank storing and retrieving the image in response to the image processing instruction;

where the processing element associated with each processing bank directly read from

and store to the local buffers of an adjacent processing bank, if any;

each processing bank receiving an image from the programmable input addresser via the first set of local buffers, each processing bank also receiving the image from an input block addresser via the second set of local buffers, each processing bank outputting the processed image to the programmable output addresser via the third set of local buffers, each bank also sending the processed image to the programmable output addresser via the fourth set of local buffers;

where the image processing instruction include an instruction that selectively designate one of the group consisting of the first level and the second level to receive the image from the programmable input block addresser as a selected input level, and a non-selected input level, such that simultaneously the selected input level receives the image while the processing element processes the image from the non-selected input level;

where the image processing instruction include an instruction that selectively designate one of the group consisting of the third level and the fourth level to output the processed image to an output block addresser as a selected output level, and a non-selected output level, such that simultaneously the selected output level sends the processed image data while the processing element processes the image from the non-selected output level; and

the programmable output addresser to receive the processed image from the selected output level, the output block addresser to output the processed image in accordance with a programmed predefined output pattern.

Claim 34 (original): The image transform processor of claim 33 further comprising:

a Huffman decoder that decodes a encoded image into the image prior to sending the image to the SIMD processor; and

a Huffman encoder that encodes the image from the SIMD processor.

Claim 35 (original): The image transform processor of claim 34 further comprising:

one or more Huffman control registers that causes the Huffman decoder to receive the encoded image, decode the encoded image to produce the image, and to provide the image to the SIMD processor, and that causes the Huffman encoder to receive the processed image from the SIMD processor, encode the processed image and output the encoded processed image.

Claim 36 (original): The image transform processor of claim 33 wherein the SIMD processor further comprises:

a boolean accumulator that has a boolean flag, the controller having a conditional write instruction that overwrites a value in the local buffers based on a state of the boolean flag.

Claim 37 (original): The image transform processor of claim 33, wherein each processing element includes a boolean accumulator that has a boolean flag, the controller causing the processing element to store a result of a comparison operation in the respective boolean flag.

Claim 38 (original): The image transform processor of claim 33 wherein the SIMD processor further comprises:

a base pointer register that stores a base address (BA);

a horizontal counter configuration register that stores a horizontal count (Hcount);

a vertical counter configuration register that stores a vertical count (V count); and

a row configuration register that stores the length a row (Hdim), where the controller is responsive to an instruction that specifies a horizontal offset (Hoft) and a vertical offset (Voft), the controller generating an effective two-dimensional address (EA) to the input buffers and the output buffers in accordance with the following relationship:

EA =BA +((V count+ V oft)*Hdim)+(Hcount+Hofi).

Claim 39 (original): The image transform processor of claim 33 further comprising:

an auxiliary bank including:

one local buffer of the first set of local buffers;

one local buffer of the second set of local buffers; and

one local buffer of the third set of local buffers, where the auxiliary bank is adjacent an end processing bank of the processing banks, the end processing bank directly reads data from and stores data to the local buffers of the auxiliary bank.

Claim 40 (original): An image transform processor comprising:

a programmable input block addresser to retrieve image data in accordance with a first programmed predefined access pattern as retrieved image data;

a SIMD processor including a controller coupled to a memory storing a image processing instruction, the SIMD processor having processing elements and local buffers arranged in levels and processing banks, each processing bank being connected in parallel with other processing banks, the controller being coupled to each processing element and local buffer to control the operation of each processing element and local buffer such that the processing banks simultaneously respond to the same instruction from the controller,

the SIMD processor being arranged as:

(i) a first level including a first set of local buffers;

(ii) a second level including a second set oflocal buffers;

(iii) a processing level including a set of processing elements that generates processed image data from image data stored in the local buffers in accordance with the image processing instructions;

(iv) a third level of a third set of local buffers;

(v) a fourth level of a fourth set of local buffers;

a programmable input buffer controller to store the retrieved image data in a specified level of the local buffers in accordance with a second programmed predefined access pattern;

where in the SIMD processor:

each bank including one local buffer of the first set of local buffers, one local buffer of the second set of local buffers, one processing element from a set of processing elements, one local buffer of the third set of local buffers, and one local buffer of the fourth set of local buffers, the processing element of each bank storing and retrieving image data from the local buffers in response to the instructions;

where the processing elements of the processing banks directly read data from and store data to the local buffers of an adjacent processing bank, if any;

each bank receiving image data from the input block addresser via the first set of local buffers, each bank also receiving image data from the input block addresser via the second set of local buffers, each bank outputting the processed image data to the output block addresser via the third set of local buffers, each bank also sending the processed image data to the output block addresser via the fourth set of local buffers;

where the image processing instructions include instructions that selectively designate one of the group consisting of the first level and the second level to receive image data from the input block addresser as a selected input level, the other level being a non-selected input level, such that simultaneously the selected input level receives image data while the processing element processes image data from the non-selected input level; and

where the image processing instructions include instructions that selectively designate one of the group consisting of the third level and the fourth level to output the processed image data to the output block addresser as a selected output level, the other level being a non-selected output level, such that simultaneously the selected output level sends the processed image data while the processing element processes image data from the non-selected output level; and

a programmable output buffer controller to cause the local buffers of the selected output level to output the processed image in accordance with a third programmed predefined access pattern as output image data; and

a programmable output block addresser to generate addresses to output the output image data in accordance with a fourth predefined access pattern.

Claims 41-43 (cancelled).

Claim 44 (previously presented): An image transform processor for processing image data, comprising:

a means capable of receipt of the image data from a data source over a data path and processing the digital image data; and

a means that controls transfer of the image data from the data source to a programmable arithmetic processing means by providing a source address onto a source address path, the source address identifying the data source, the programmable arithmetic processing means comprising a first set of local buffers and a second set of local buffers, each buffer in the first set of local buffers alternately used for fetching input image data and each buffer in the second set of local buffers alternately used for storing output image data.

Claim 45 (original): The image transform processor of claim 44 further comprising:

a means for controlling transfer of the image data from the programmable arithmetic processor to a memory by providing a write address onto a write path, the write address identifying a write address in the memory for storage of the digital image data.

Claim 46 (previously presented): An image transform processor for processing image data, the image transform processor comprising:

a means capable of receiving the image data from a memory over a data bus coupled between a programmable arithmetic processing means and the memory and processing the image

data; and

a means for controlling transfer of the digital image data from the memory to the programmable arithmetic processing means by:

(i) means for providing a memory address onto a read address bus coupled between a programmable input addressing means and the memory, the memory address identifying a location of the image data within the memory, and

(ii) means for providing a storage address to the programmable arithmetic processing means, the storage address identifying a local buffer within the programmable arithmetic processing means for storage of the image data, the programmable arithmetic processing means comprising a first set of local buffers and a second set of local buffer, each buffer in the first set of local buffers alternately used for fetching input image data and each buffer in the second set of local buffers alternately used for storing output image data.